

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

..designed for general-purpose power amplifier and switching applications.

FEATURES:

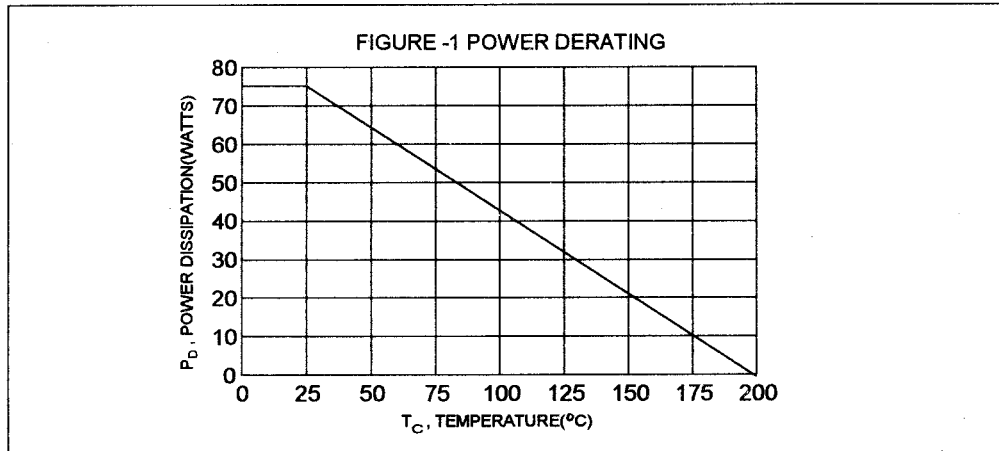
- * Low Collector-Emitter Saturation Voltage
 $V_{CE(sat)} = 0.7 \text{ V (Max.) @ } I_C = 1.5 \text{ A}$
- *Excellent DC Current Gain
 $hFE = 25-100 @ I_C = 1.5 \text{ A}$
- * Low Leakage Current- $I_{CEX} = 0.1 \text{ mA(Max)}$

MAXIMUM RATINGS

Characteristic	Symbol	2N4231A 2N6312	2N4232A 2N6313	2N4233A 2N6314	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	V
Collector-Base Voltage	V_{CBO}	40	60	80	V
Emitter-Base Voltage	V_{EBO}	5.0			V
Collector Current-Continuous -Peak	I_C I_{CM}	5.0 10			A
Base Current	I_B	2.0			A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.43			W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	- 65 to +200			$^\circ\text{C}$

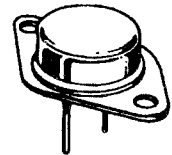
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	2.32	$^\circ\text{C/W}$

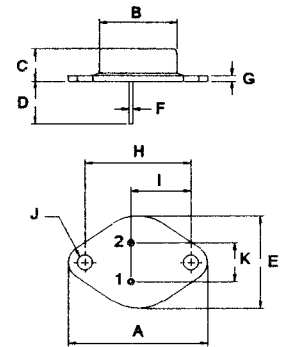


NPN	PNP
2N4231A	2N6312
2N4232A	2N6313
2N4233A	2N6314

5 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTOR
40-80 VOLTS
75 WATTS



TO-66



PIN 1. BASE
2. EMITTER
COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	30.60	32.52
B	13.85	14.16
C	6.54	7.22
D	9.50	10.50
E	17.26	18.46
F	0.76	0.92
G	1.38	1.65
H	24.16	24.78
I	13.84	15.60
J	3.32	3.92
K	4.86	5.34

2N4231A Thru 2N4233A NPN / 2N6312 Thru 2N6314 PNP

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector - Emitter Sustaining Voltage (1) ($I_c = 100\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	40 60 80		V
Collector Cutoff Current ($V_{CE} = 30\text{ V}$, $I_B = 0$) ($V_{CE} = 50\text{ V}$, $I_B = 0$) ($V_{CE} = 70\text{ V}$, $I_B = 0$)	I_{CEO}		1.0 1.0 1.0	mA
Collector-Emitter Leakage Current ($V_{CE} = 40\text{ V}$, $V_{BE(off)} = 1.5\text{ V}$) ($V_{CE} = 60\text{ V}$, $V_{BE(off)} = 1.5\text{ V}$) ($V_{CE} = 80\text{ V}$, $V_{BE(off)} = 1.5\text{ V}$) ($V_{CE} = 40\text{ V}$, $V_{BE(off)} = 1.5\text{ V}$, $T_c = 125^\circ\text{C}$) ($V_{CE} = 60\text{ V}$, $V_{BE(off)} = 1.5\text{ V}$, $T_c = 125^\circ\text{C}$) ($V_{CE} = 80\text{ V}$, $V_{BE(off)} = 1.5\text{ V}$, $T_c = 125^\circ\text{C}$)	I_{CEX}		0.1 0.1 0.1 1.0 1.0 1.0	mA
Collector Cutoff Current ($V_{CB} = 40\text{ V}$, $I_E = 0$) ($V_{CB} = 60\text{ V}$, $I_E = 0$) ($V_{CB} = 80\text{ V}$, $I_E = 0$)	I_{CBO}		50 50 50	μA
Emitter Cutoff Current ($V_{EB} = 5.0\text{ V}$, $I_C = 0$)	I_{EBO}		0.5	mA

ON CHARACTERISTICS (1)

DC Current Gain ($I_c = 0.5\text{ A}$, $V_{CE} = 2.0\text{ V}$) ($I_c = 1.5\text{ A}$, $V_{CE} = 2.0\text{ V}$) ($I_c = 3.0\text{ A}$, $V_{CE} = 2.0\text{ V}$) ($I_c = 5.0\text{ A}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	40 25 10 4.0	100	
Collector-Emitter Saturation Voltage ($I_c = 1.5\text{ A}$, $I_B = 0.15\text{ A}$) ($I_c = 3.0\text{ A}$, $I_B = 0.3\text{ A}$) ($I_c = 5.0\text{ A}$, $I_B = 1.25\text{ A}$)	$V_{CE(sat)}$		0.7 2.0 4.0	V
Base-Emitter Saturation Voltage ($I_c = 1.5\text{ A}$, $V_{CE} = 2.0\text{ V}$)	$V_{BE(on)}$		1.4	V

DYNAMIC CHARACTERISTICS

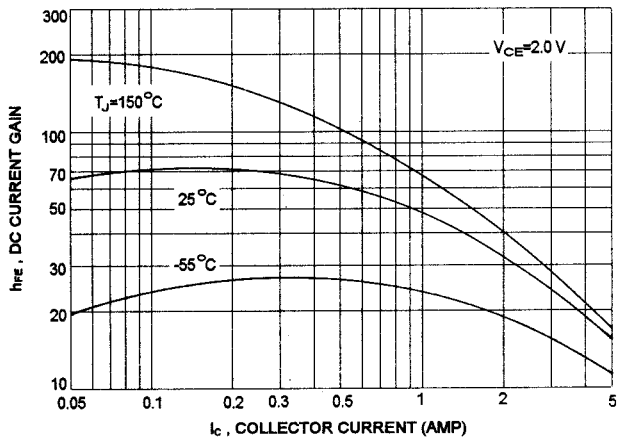
Current Gain - Bandwidth Product (2) ($I_c = 0.5\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ MHz}$)	f_T	4.0		MHz
Output Capacitance ($V_{CB} = 10\text{ V}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}		300	pF
Small-Signal Current Gain ($I_c = 0.5\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ KHz}$)	h_{fe}	20		

(1) Pulse Test: Pulse width = 300 μs , Duty Cycle $\leq 2.0\%$

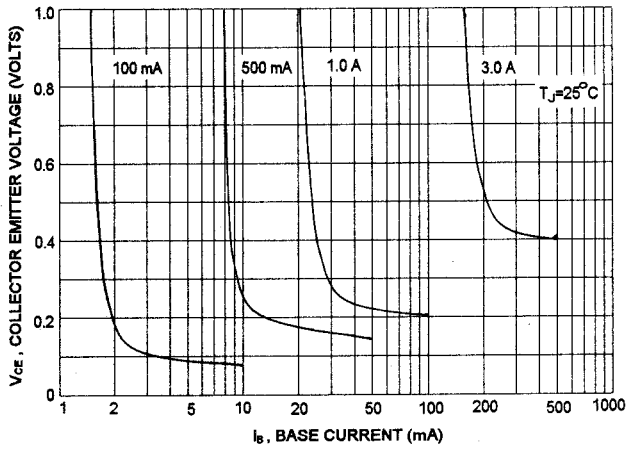
(2) $f_T = |h_{fe}| \cdot f_{test}$

NPN 2N4231A thru 2N4233A

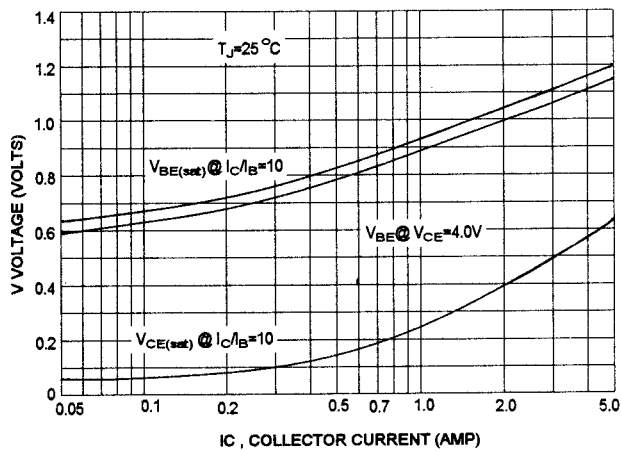
DC CURRENT GAIN



COLLECTOR SATURATION REGION

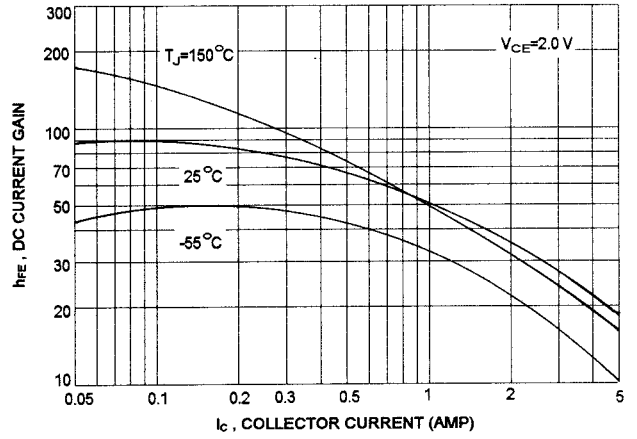


"ON" VOLTAGES

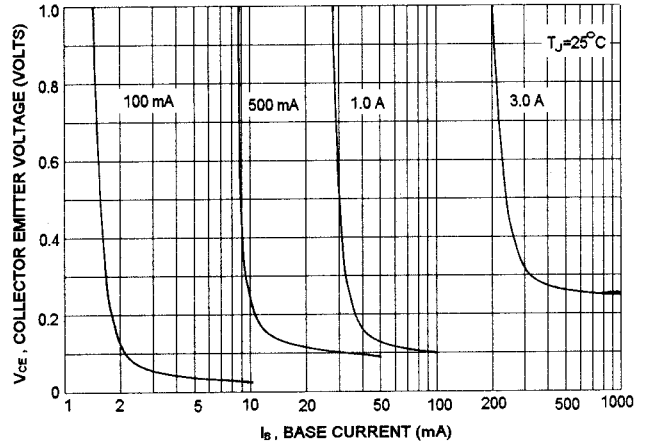


PNP 2N6212 thru 2N6314

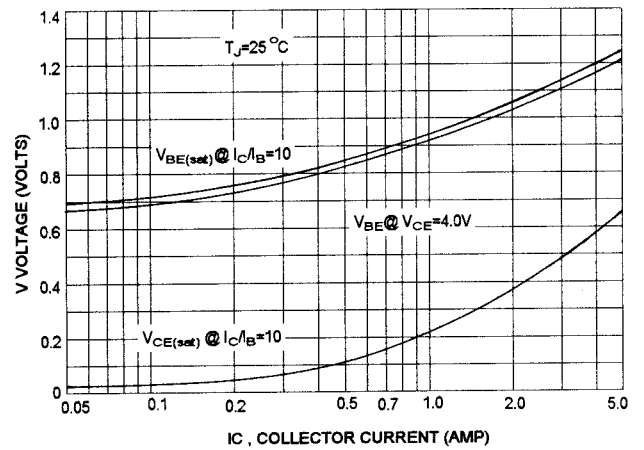
DC CURRENT GAIN



COLLECTOR SATURATION REGION

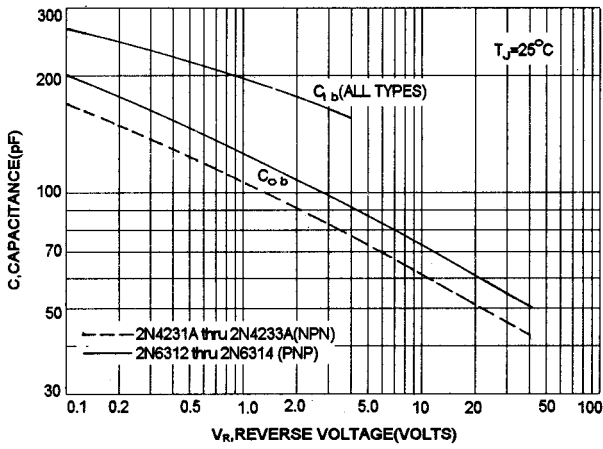


"ON" VOLTAGES

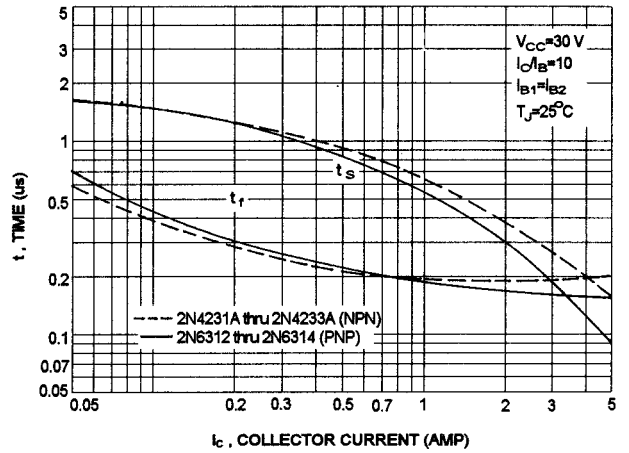


2N4231A thru 2N4233A NPN / 2N6312 thru 2N6314 PNP

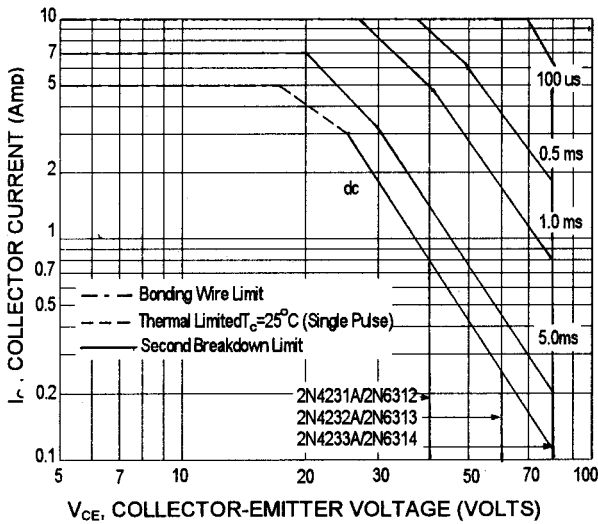
CAPACITANCES



TURN-OFF TIME



ACTIVE-REGION SAFE OPERATING AREA (SOA)



There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_c - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on $T_{J(PK)} = 200^\circ\text{C}$; T_c is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 200^\circ\text{C}$. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.